REMARKS

By this amendment, claims 11, 22, 34, and 35 have been amended. Accordingly, claims 1-35 are pending in the present application. The claim amendments are supported by the specification, the accompanying figures, and claims as originally filed, with no new matter being added. In particular, support for the amendments can be found in Figure 8. The specification has been amended to update the priority data and to correct typographical errors. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

1. Rejection Under the Judicially Created Doctrine of Double Patenting

Claims 1-35 have been rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-32 of U.S. Patent No. 6,107,183 to Sandhu et al. (hereinafter "*Sandhu*") for the reasons set forth on page 4 of the Office Action.

This rejection will be addressed when allowable subject mater has been indicated by the Examiner.

2. Rejections Under 35 U.S.C. §103

Claims 1-35 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,445,996 to Kodera et al. (hereinafter "*Kodera*") in view of U.S. Patent No. 5,708,303 to Jeng and U.S. Patent No. 5,486,493 to Jeng, collectively "the *Jeng* patents," for the reasons set forth on pages 2-4 of the Office Action. Applicants respectfully traverse.

As stated in the present application with respect to the problem of fringe capacitance that is overcome by the present invention:

> The electric field formed by a potential difference applied across an adjacent pair of lines of conductive material 16 is strongest in a direct line and centrally between the adjacent pair, such as along dashed line N in Figure 2. But the electric field so formed also extends to a fringe area not in a direct line between the adjacent pair, such as along dashed line F in Figure 2. The field in this area, called the fringe, is associated with a portion of the total capacitance, the portion called herein "fringe capacitance," between the adjacent pair.

Specification at page 10, lines 6-11. In order to overcome the above problem of fringe capacitance, both above and below a direct line between the paired lines of conductive material, the present invention extends the low dielectric constant material both above and below the upper and lower surface of the paired lines of conductive material. In order to accomplish the low dielectric constant material layer extending below the bottom layer of each conductive line, the step of etching requires: "etching through said additional layer and said conductive layer *and into said first dielectric layer*," as recited in present claims 1, 11, 22, 34, and 35, and "leaving a space between adjacent remaining portions of said conductive layer that *extends below the lower surface of said conductive layer*" as recited in some form in present independent claims 11, 22, 34, and 35. (emphasis added)

In contrast, Kodera does not teach a dielectric material layer extending below the bottom surface of a conductive layer, does not teach the use of low dielectric constant materials, does not address the problem of fringe capacitance, and in fact clearly illustrates a failure to comprehend, appreciate, or design for a solution to the problem of fringe capacitance.

Kodera teaches, as seen in Figure 30C, a dielectric material 217 in spaces between adjacent conductive material 222 that has a top surface that is above the top surface of the conductive material 222 and a bottom surface that is on a level with the bottom surface of conductive material 222. Again, *Kodera* also teaches, as seen in Figure 33J, a dielectric material 246 in spaces between adjacent conductive material 203 that has a top surface that is above the top surface of conductive

material 246 and a bottom surface that is on a level with the bottom surface of conductive material 246.

These two examples clearly illustrate that *Kodera* does not comprehend, appreciate, or design for a solution to the problem of fringe capacitance. Rather, *Kodera* seeks to improve a polishing operation on the upper surface of the dielectric layers 217, 246. In particular, *Kodera* uses a spacer layer to create a polishing stop. Although this creates a final product with a dielectric layer that extends higher than the adjacent conductor layer, this does address the problem of fringe capacitance. When the structures taught by *Kodera* are compared to Figure 2 of the present application, the differences are pronounced. For example, reference numeral F within dielectric material 17 in Figure 2 of the present application illustrates a solution produced by the inventive method that is not taught, suggested, or implied by the teaching of *Kodera*. In addition, *Kodera* does not teach the use of low k dielectric materials.

Hence, there is nothing in *Kodera* that would teach or suggest either: (1) selecting an etch process that would extend into the lower dielectric layer 202; or (2) depositing a low k dielectric layer between conductive lines to reduce fringe capacitance.

Neither of the *Jeng* patents are properly combinable with *Kodera* to obviate the presently recited claims. In particular, the methods disclosed are diametrically opposite. The *Jeng* patents involve reduction of cross talk using a damascene process where the dielectric is first deposited (low dielectric constant or otherwise) and the dielectric trenches are then etched where the metal is to be deposited. In contrast, Kodera involves an improved polishing method using the process of forming metal lines first and then putting the dielectric in between. Thus, the *Jeng* patents disclose: (1) a different object than *Kodera*, and (2) a completely different process than *Kodera*. Hence, there is no

reason or motivation that would influence one skilled in the art practicing *Kodera* to look to the *Jeng* patents for any reason and the processes are therefore not combinable.

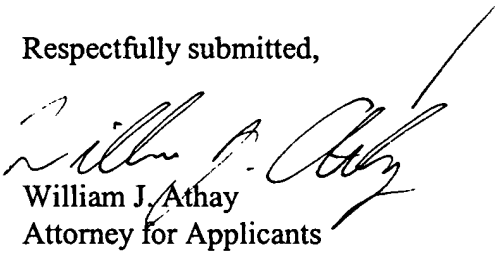
Accordingly, Applicants therefore respectfully request that the rejection of the claims under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the present claims. In the event the Examiner finds any remaining impediment to the prompt allowance of this application that could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 4th day of March 2002.

Respectfully submitted,



William J. Athay
Attorney for Applicants
Registration No. 44,515

WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111
Telephone: (801) 533-9800
Fax: (801) 328-1707

VERSION WITH MARKINGS SHOWING THE CHANGES MADE

In the specification:

The paragraph beginning at page 2, line 2 has been amended as follows:

This application is a divisional of application serial number 09/249,659, filed on February 12, 1999, now U.S. Patent No. 6,107,686, which is a divisional application of serial number 08/677,514, filed on July 10, 1996, now U.S. Patent No. 6,107,183, [titled Interlevel Dielectrics and Methods for Forming the Same,] both of which are incorporated herein by reference.

The paragraph beginning at page 3, line 9 has been amended as follows:

One way to decrease unneeded capacitance between metal lines in an integrated circuit is to decrease the dielectric constant of the material between them. Silicon dioxide, the material of choice for interlevel dielectrics, has a relatively high dielectric constant. Replacing silicon dioxide with a material having a lower dielectric constant would thus provide reduced capacitance. Useable materials having a low dielectric constant (e.g. less than about 3.6.) are generally much less stable than silicon dioxide and are thus unable to reliably protect the metal lines, and are unable to withstand further processing.

The paragraph beginning at page 3, line 16 has been amended as follows:

One way to gain some of the benefits of low dielectric constant materials is shown in Figure 1. Figure 1 is a partial cross section of a partially formed integrated circuit device. A substrate or lower layer 12 has a first dielectric layer 14 comprised of a traditional dielectric material such as silicon dioxide. Lines of conductive material 16, typically metal, overlie first dielectric layer 14. A material with a dielectric constant lower than that of silicon dioxide 18 is located in between lines of conductive material 16. Lines of conductive material 16 together with low dielectric constant dielectric material 18 are covered by a second dielectric layer 21 comprised of a traditional dielectric material such as silicon dioxide. Second dielectric layer 21 together with first dielectric layer 14 isolate low dielectric constant dielectric material 18 from other portions of the integrated [integrate] circuit. Second dielectric layer 21 allows further processing, including formation of contact holes for contacting lines of conductive material 16 such as contact hole 46, without exposing dielectric material 18 to processing agents.

The paragraph beginning at page 5, line 2 has been amended as follows:

In accordance with the present invention, an interlevel dielectric structure includes first and second dielectric layers between which are located lines of a conductive material with a dielectric material in spaces between the lines of conductive material, with the lower surface of the dielectric material extending lower than the lower surface of lines of conductive material adjacent thereto, and the upper surface of the dielectric material extending higher than the upper surface of lines of conductive material adjacent thereto, thus reducing fringe and total capacitance between the lines of conductive material. The dielectric material, which has a dielectric constant of less than about 3.6, does not extend directly above the upper surface of the lines of conductive material, allowing formation of subsequent contacts down to the lines of conductive material without exposing the dielectric material to further processing.

In the claims:

Claims 11, 22, 34, and 35 have been amended as follows:

11. (Once Amended) A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situates on a semiconductor wafer;

depositing a conductive layer on said first dielectric layer, the conductive layer having a lower surface;

patterning said conductive layer by:

forming a mask layer on said conductive layer;[,] and

etching through said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer that extends below the lower surface of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material each having an upper surface;

depositing an additional layer on the upper surfaces of lines of conductive material and on said first dielectric layer;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

22. (Once Amended) A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a metal layer on said first dielectric layer, the metal layer having a lower surface;

patterning said metal layer by:

forming a mask layer on said metal layer;[,] and

etching through said metal layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said metal layer that extends below the lower surface of said metal layer, said adjacent remaining portions of said metal layer forming metal lines each having an upper surface;

depositing a thin layer of silicon dioxide conformably over said metal lines and selectively on said upper surfaces of said metal lines;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

34. (Once Amended) A method of forming an interlevel dielectric comprising:

providing a first dielectric layer over a surface of a substrate;

forming a conductive layer on said first dielectric layer, the conductive layer having a lower surface;

forming an additional layer on said conductive layer;

forming lines of conductive material having spaces therebetween that extend below the lower surface of said conductive layer from the conductive layer;

filling the spaces between the lines of conductive material with dielectric material having a dielectric constant of less than about 3.6; and

forming a second dielectric layer on the additional layer.

35. (Once Amended) A method of forming an interlevel dielectric comprising:

providing a first dielectric layer over a surface of a substrate;

forming a conductive layer on said first dielectric layer, the conductive layer having a lower surface;

forming an additional layer on said conductive layer;

etching through said additional layer and said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer that extends below the lower surface of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material;

filling the spaces between adjacent remaining portions of said conductive layer with dielectric material having a dielectric constant of less than about 3.6; and

forming a second dielectric layer on the additional layer.